Amendments to the specification:

Please replace paragraph [0023] with the following revised paragraph:

The invention also relates to a pipeline arrangement for a network traffic scheduler. The pipeline comprises a hierarchical structure, a plurality of SRAM and DRAM memory devices external to the scheduler, and control blocks of scheduling elements stored in said memory devices with at least some of the memory devices storing more than one type of control block. The SRAM memory is used if the content of a control block is Read-Modify-Write at packet enqueue and at dequeue. The SRAM and DRAM memory are used, with the DRAM being preferred, if the control block content is Read-Modify-Write only, at the packet dequeue. The DRAM memory is used if the control block content is 'read' only at packet enqueue and dequeue. The control blocks include flow queue control blocks, frame control flow blocks, hierarchy control blocks, target port queue control blocks, ~~hierarchy control blocks~~ and schedule control blocks. The hierarchical structure comprises a physical port bandwidth that is divided into a plurality of logical links, the bandwidth available to each of the logical links is divided into a plurality of VLANs, and the bandwidth associated with each VLAN is shared by a plurality of individual user flows. The pipeline also includes non-hierarchical link sharing whereby physical port bandwidth resources are shared among individual traffic flows.